09-29-00

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SKJERVEN MORRILL MACPHERSON LLP

Docket No.: M-8847 US

09/27/00 PTO 0868 U.S.

September 27, 2000

Box Patent Application
Commissioner For Patents
Washington, D. C. 20231

09/672131 U.S. PTO 09/27/00 JC675

Enclosed herewith for filing is a patent application, as follows:

Inventor(s): Gary S. Kitten and Anthony B. Armstrong

Title: Mechanism To Disable Dynamically A Computer Audio Input/Output Connector

X Return Receipt Postcard
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8 page(s) Specification (not including claims)
3 page(s) Claims
1 page Abstract
3 Sheet(s) of Drawings
3 page(s) Declaration For Patent Application and Power of Attorney

CLAIMS AS FILED

For	Number Filed			Number Extra		Rate			Basic Fee $690.00
Total Claims	16	-20	=	0	x	$18.00	=	$	0.00
Independent Claims	3	-3	=	0	x	$78.00	=	$	0.00
☐ Fee of ____ for the first filing of one or more multiple dependent claims per application								$	
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MECHANISM TO DISABLE DYNAMICALLY A COMPUTER AUDIO INPUT/OUTPUT CONNECTOR

Gary S. Kitten
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BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to audio connectors, and more particularly to an apparatus and method for significantly reducing spurious noise coupled onto one audio input/output ("I/O") connector and preventing such spurious noise from interfering with a signal from another audio I/O connector.

Description of the Related Art

Computer systems in general and personal computer systems in particular have attained widespread use for providing computer power to many segments of today's modern society. A personal computer system can usually be defined as a desktop, floor standing, or portable microcomputer that includes a system unit having a system processor and associated volatile and non-volatile memory, a display monitor, a keyboard, one or more removable storage devices, a fixed drive storage device, and an optional printer. One of the distinguishing characteristics of these systems is the use of a system board to connect these components together electronically. These personal computer systems are designed primarily to provide independent computing power to a single user (or to a relatively small group of users in the case of personal computers that serve as computer server systems) and are inexpensively priced for purchase by individuals or small businesses. A personal computer system may also include one or more of a plurality of I/O devices (*i.e.*, peripheral devices) that are coupled to the system processor and that perform

specialized functions. Examples of peripheral devices include modems, sound and video devices, or specialized communication devices. Mass storage devices such as hard disks, compact disk read only memory ("CD-ROM") drives, and magneto-optical drives are also considered to be peripheral devices. Computers capable of producing sound effects are in increasing demand as computers are used for business applications, artistic endeavors, entertainment, and education. Computers requiring audio inputs through devices such as microphones are in increasing demand as computers are used for applications requiring audio data inputs (*e.g.*, dictation programs, video conferencing, Voice over Internet Protocol ("VoIP"), and voice recognition programs).

Computer systems today often include audio controllers (*e.g.*, sound cards) to which audio I/O peripheral devices (*e.g.*, microphones and speaker systems) can be attached for the input or output and processing of signals representing sound. Most computer systems provide hardware audio I/O connectors such as jacks (*i.e.*, connectors designed to receive plugs) via which such audio peripheral devices can be connected to the computer system's audio controller or integrated audio solution. Primary audio I/O connectors are often located at the back of a computer system to allow coupling of devices on a more permanent basis without crowding the work area at the front of the computer system. Secondary audio I/O connectors may be located on or near the front of a computer system to make them more accessible to users.

References to audio controllers and other integrated audio solutions, audio I/O connectors, and audio devices specifically include audiovisual controllers and other integrated audiovisual solutions, audiovisual I/O connectors, and audiovisual devices.

This placement of audio I/O connectors often gives rise to spurious noise coupled onto a primary audio I/O connector and its associated electrical components and cabling. This noise may be troublesome at any time, but particularly when a device is coupled to a secondary audio I/O connector. If this noise coupled onto the primary audio I/O connector is not significantly reduced, it is processed with, and in that sense interferes with, the signal associated with a device coupled to a secondary

audio I/O connector, reducing the quality of the input or output from the device coupled to the secondary audio I/O connector. A challenge presented by this situation is the effective and inexpensive significant reduction of the spurious noise. One method of reducing this noise involves simply grounding the primary audio I/O connector when a device is coupled to a secondary I/O connector. This method, depending on the physical location of the coupling of the primary audio I/O connector to ground, may still allow the coupling of some spurious noise onto the primary audio I/O connector. Another method of reducing spurious noise coupled onto a primary audio I/O connector is to open the connection to the primary audio I/O connector when a device is coupled to a secondary I/O connector. The switches required for this, however, are manufactured in multiple units to a pack, making this method expensive to implement. Another method of reducing spurious noise coupled onto a primary audio I/O connector is to shield the connectors and their associated electrical components and cabling, but adequate shielding is also expensive to implement.

SUMMARY OF THE INVENTION

The present invention relates to a method of dynamically disabling a primary audio I/O connector when a device is connected to a secondary audio I/O connector and locating the disablement point to significantly reduce any spurious noise coupled onto the primary audio I/O connector and its associated electrical components and cabling. In one embodiment, a transistor disables a primary audio I/O connector by pulling it to a zero voltage level when a device is coupled to an secondary audio I/O connector.

In another embodiment, a direct-current ("DC") blocking cap is included with the disabling device to prevent spurious noise from bleeding through the circuit.

In another embodiment, a mechanical switch detects the coupling of an audio I/O device coupled to a secondary audio I/O connector and disables a primary audio I/O connector.

One advantage of the present invention is that transistors are relatively inexpensive electronic components and can be purchased singly. Another advantage of the present invention is that a transistor provides a low resistance from the primary audio cable to ground, ensuring that the cable is thoroughly grounded and significantly reducing the interference coupled onto the primary audio I/O connector and its associated electrical components and cabling.

An improvement to the reduction of spurious noise coupled onto a primary audio I/O connector is desirable that is more effective and less expensive than the methods now in use.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

Figure 1 is a block diagram of a typical computer system with which the present invention may be used.

Figure 2 is a functional block diagram of an exemplary computer audio circuit with which the present invention can be used, including an embodiment of the present invention.

Figure 3 is a circuit diagram of an exemplary computer audio circuit with which the present invention can be used, including an embodiment of the present invention.

The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

The following sets forth a detailed description of a mode for carrying out the invention. The description is intended to be illustrative of the invention and should not be taken to be limiting.

Figure 1 is a block diagram of an exemplary computer system 100 that may be found in many forms, including, for example, mainframes, minicomputers, workstations, servers, personal computers, internet terminals, notebooks, and embedded systems. Personal computer ("PC") systems, such as those compatible with the x86 configuration, include desktop, floor standing, or portable versions. A typical PC system 100 is a microcomputer that includes a microprocessor (or simply "processor") 110, associated main memory 150 and control logic and a number of peripheral devices that provide I/O for the system 100. Exemplary computer system 100 is powered by a power supply 114 with voltage regulator 115. The peripheral devices often include keyboards 191, mouse-type input devices 192, and other traditional I/O devices (not shown) that may include display monitors, floppy and hard disk drives, CD-ROM drives, modems, and printers. The number of I/O devices being added to personal computer systems continues to grow. For example, many computer systems also include terminal devices, televisions, sound devices, voice recognition devices, electronic pen devices, and mass storage devices such as tape drives, or digital video disks ("DVDs"). The peripheral devices usually communicate with the processor over one or more peripheral component interconnect ("PCI") slots 166, universal serial bus ("USB") ports 175, or integrated device electronics ("IDE") connectors 176. The PCI slots 166 may use a card/bus controller 165 to connect to one or more buses such as host bus 120, PCI bus160, and low pin count ("LPC") bus 180, with the buses communicating with each other through the use of one or more hubs such as graphics controller memory hub 140 and I/O controller hub 170. Typical systems such as exemplary system 100 often include network interface cabling slots 198 to accommodate network cards that mediate between the computer and the physical media over which transmissions to and from system 100 travel. The USB ports 175 and IDE connectors 176 may connect to one or more of the hubs 140,

170. The hubs may communicate with each other through the use of one or more links such as hub link 190. Many I/O devices can also be accommodated by parallel ports 193 and serial ports 194 that are coupled to an I/O controller 187 that is in turn coupled to a LPC bus 180. Typical computer systems often include a graphics card 130 coupled to a graphics memory controller hub 140 by a graphics bus 135 and a main memory 150 coupled to a graphics memory controller hub 140 by a system management ("SM") bus 130. Finally, a typical computer system also includes software modules known as the basic input/output system (BIOS). The BIOS code 184 is usually stored on the firmware hub 186 in memory 183.

Exemplary computer system 100 in Figure 1 includes a primary audio I/O connector 145 and a secondary audio I/O connector 195 to which audio I/O devices can be coupled to connect them to the audio controller 155, and transistor 146 pulls a device coupled to primary audio I/O connector 145 to a substantially zero voltage level when a device is coupled to secondary audio I/O connector 195. A first embodiment of the present invention is represented conceptually in Figure 1 as a transistor 146 coupled to connectors 145 and 195 and ground.

In the present invention, a transistor may be conceptualized as having a control terminal that controls the flow of current between a first current handling terminal and a second current handling terminal. An appropriate condition on the control terminal causes a current to flow from/to the first current handling terminal and to/from the second current handling terminal. In a bipolar NPN transistor, the first current handling terminal is the collector, the control terminal is the base, and the second current handling terminal is the emitter. A sufficient current into the base causes a collector-to-emitter current to flow. In a bipolar PNP transistor, the first current handling terminal is the emitter, the control terminal is the base, and the second current handling terminal is the collector. A current exiting the base causes an emitter-to-collector current to flow.

A FET may likewise be conceptualized as having a control terminal that controls the flow of current between a first current handling terminal and a second

current handling terminal. Although FETs are frequently discussed as having a drain, a gate, and a source, in most such devices the drain is interchangeable with the source. This is because the layout and semiconductor processing of the transistor is symmetrical (which is typically *not* the case for bipolar transistors). For an N-channel FET, the current handling terminal normally residing at the higher voltage is customarily called the drain. The current handling terminal normally residing at the lower voltage is customarily called the source. A sufficient voltage on the gate causes a current to therefore flow from the drain to the source. The gate-to-source voltage referred to in an N-channel FET device equations merely refers to whichever diffusion (drain or source) has the lower voltage at any given time. To reflect the symmetry of most N-channel FETs, the control terminal is the gate, the first current handling terminal may be termed the "drain/source," and the second current handling terminal may be termed the "source/drain." Such a description is equally valid for a P-channel FET, since the polarity between drain and source voltages, and the direction of current flow between drain and source, is not implied by such terminology. Alternatively, one current handling terminal may be arbitrarily deemed the "drain" and the other deemed the "source," with an implicit understanding that the two are not distinct, but interchangeable.

Referring to Figure 2, a functional block diagram of a circuit 200, an exemplary computer audio circuit with two inputs or outputs, is shown. Circuit 200 comprises disabling device 210 and circuit element 227, which, taken together, represent a second embodiment of the present invention. Circuit element 227 couples filter circuit 220 with inverting amplifier 230 and serves as a DC blocking cap. Exemplary circuit 200 further comprises a filter circuit 220, an inverting amplifier 230, and an integrating amplifier 240. Exemplary circuit 200 further comprises primary audio I/O coupling 250, secondary audio I/O coupling 255, audio input reference voltage coupling 260, audio input power coupling 265, microphone bias supply coupling 266, and primary audio input disable signal coupling 213. Exemplary circuit 200 further comprises circuit element 281, which couples audio input reference voltage coupling 260 to circuit element 227 and inverting amplifier 230 at a point in circuit 200 disposed between circuit element 227 and integrating

amplifier 230. Exemplary circuit 200 further comprises audio I/O coupling 270, which couples exemplary circuit 200 to the remainder of exemplary computer system 100.

Referring to Figure 3, a circuit diagram of a circuit 300, an exemplary computer audio circuit with two inputs, is shown. Circuit 300 comprises disabling device 210 and circuit element 227, which, taken together, represent a second embodiment of the present invention. Disabling device 210 comprises circuit element 212 and FET 211 where the drain is coupled to primary audio input coupling 250, the source is coupled to ground, and the gate is coupled to primary audio input disable signal coupling 213. Filter circuit 220 comprises circuit elements 221, 222, 223, 224, 225, 226 and 228. Inverting amplifier 230 comprises circuit elements 231, 232, 233, and 234, and operational amplifier 235. Integrating filter 240 comprises circuit elements 236, 241, 242, 243, 244, and 280, and operational amplifier 245.

One skilled in the art will recognize that the foregoing components and devices in Figures 1, 2, and 3 are used as examples for the sake of conceptual clarity and that various configuration modifications are common. Consequently, as used herein the specific exemplars set forth in Figures1, 2, and 3 are intended to be representative of their more general classes. In general, use of any specific exemplar herein is also intended to be representative of its class, and the non-inclusion of such specific devices in the foregoing list should not be taken as indicating that limitation is desired.

WHAT IS CLAIMED IS:

1. An apparatus comprising:

a first audio input/output connector;

at least one second audio input/output connector;

an audio controller;

a circuit coupling the first audio input/output connector to the audio controller;

at least one circuit coupling at least one second audio input/output connector to the audio controller; and

a device electrically decoupling the first audio input/output connector from the circuit coupling the first audio input/output connector to the audio controller when an audio input/output device is coupled to at least one second input/output connector.

2. The apparatus of Claim 1, wherein the device electrically decoupling the first audio input/output connector from the circuit coupling the first audio input/output connector to the audio controller when an audio input/output device is coupled to at least one second input/output connector comprises a transistor.

3. The apparatus of Claim 2, wherein the transistor is a field effect transistor comprising a drain, a source, and a gate, wherein the drain is coupled to the first audio input/output connector, the source is coupled to ground, and the gate is coupled to at least one second audio input/output connector such that current flows into the gate when an audio input/output device is coupled to a second audio input/output connector to which the gate is coupled.

4. The apparatus of Claim 1, comprising a direct-current blocking cap, wherein the device is coupled between the direct-current blocking cap and at least one second audio input/output connector.

5. The apparatus of Claim 1, wherein the device electrically decoupling the first audio input/output connector from the circuit coupling the first audio

input/output connector to the audio controller when an audio input/output device is coupled to at least one second input/output connector comprises a mechanical switch.

6. The apparatus of Claim 1, wherein the first audio input/output connector comprises a jack.

7. The apparatus of Claim 1, wherein the second audio input/output connector comprises a jack.

8. A computer system, comprising:

a processor;

a memory coupled to the processor;

an audio controller coupled to the processor;

a first audio device input/output connector coupled to the audio controller;

at least one second audio device input/output connector coupled to the audio controller; and

a device electrically decoupling the first audio input/output connector from the circuit coupling the first audio input/output connector to the audio controller when an audio input/output device is coupled to at least one second input/output connector.

9. The computer system of Claim 8, wherein the device electrically decoupling the first audio input/output connector from the circuit coupling the first audio input/output connector to the audio controller when an audio input/output device is coupled to at least one second input/output connector comprises a transistor.

10. The computer system of Claim 9, wherein the transistor is a field effect transistor comprising a drain, a source, and a gate, wherein the drain is coupled to the first audio input/output connector, the source is coupled to ground, and the gate is coupled to at least one second audio input/output connector such that current flows into the gate when an audio input/output device is coupled to a second audio input/output connector to which the gate is coupled.

11. The computer system of Claim 8, comprising a direct-current blocking cap wherein the device is coupled between the direct-current blocking cap an at least one second audio input/output connector.

12. The computer system of Claim 8, wherein the device electrically decoupling the first audio input/output connector from the circuit coupling the first audio input/output connector to the audio controller when an audio input/output device is coupled to at least one second input/output connector is a mechanical switch.

13. The computer system of Claim 8, wherein the first audio input/output connector is a jack.

14. The computer system of Claim 13, wherein the second audio input/output connector comprises a jack.

15. The computer system of Claim 8, wherein the second audio input/output connector comprises a jack.

16. A method for disabling a computer system audio device input/output connector, the method comprising:

detecting the coupling of an audio input/output device to a first audio input/output connector; and

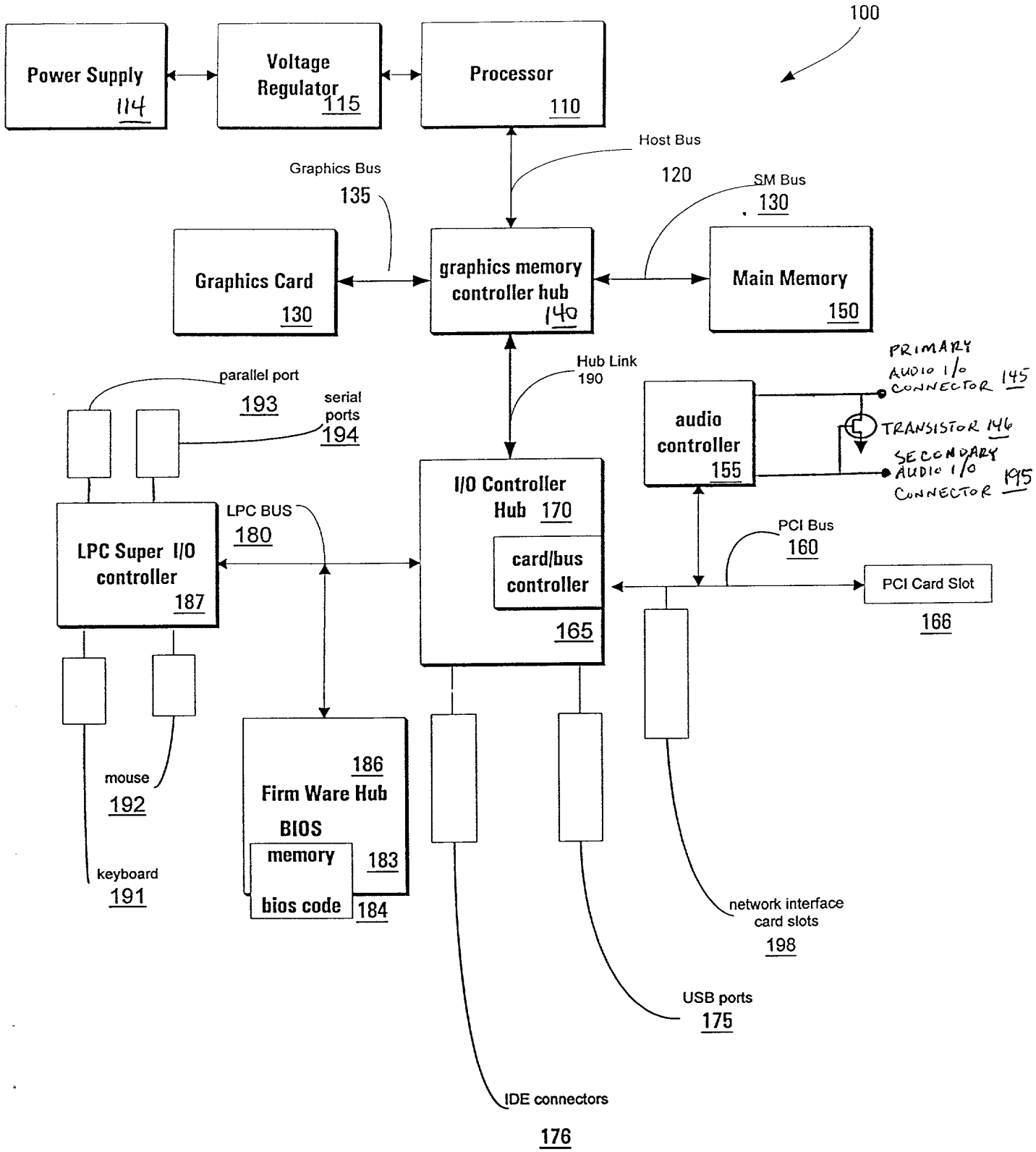
uncoupling at least one second audio input/output connector from a circuit coupling at least one second audio input/output connector to the audio controller when the coupling of an audio input/output device to the first audio input/output connector is detected.

MECHANISM TO DISABLE DYNAMICALLY A COMPUTER AUDIO INPUT/OUTPUT CONNECTOR

Gary S. Kitten
Anthony B. Armstrong

ABSTRACT OF THE DISCLOSURE

An apparatus and method are presented for dynamically disabling a first audio input/output ("I/O") connector when an audio I/O device is coupled to a second audio I/O connector, locating the disablement point to reduce significantly any spurious noise coupled onto the primary audio I/O connector and its associated electrical components and cabling. An advantage of the present invention is that it can be implemented with components that provide low resistance from the first audio I/O connector to ground, thoroughly grounding, and significantly reducing spurious noise coupled onto, the first audio I/O connector and associated electronics and cabling. This invention therefore also significantly reduces the spurious noise processed with, and therefore interfering with, the signal associated with a device coupled to a second audio I/O connector, significantly increasing the quality of the input or output signal from that secondary device. Another advantage of the present invention is that the components required are relatively inexpensive and can be purchased in single units.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Voltage Regulator
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Processor
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Host Bus
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Graphics Bus
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SM Bus
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Graphics Card
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graphics memory controller hub
140
Main Memory
150
Hub Link
190
parallel port
193
serial ports
194
audio controller
155
PRIMARY AUDIO I/O CONNECTOR 145
TRANSISTOR 146
SECONDARY AUDIO I/O CONNECTOR 195
LPC BUS
180
I/O Controller Hub 170
card/bus controller
165
PCI Bus
160
PCI Card Slot
166
LPC Super I/O controller
187
mouse
192
keyboard
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network interface card slots
198
USB ports
175
IDE connectors
176

FIG. 1

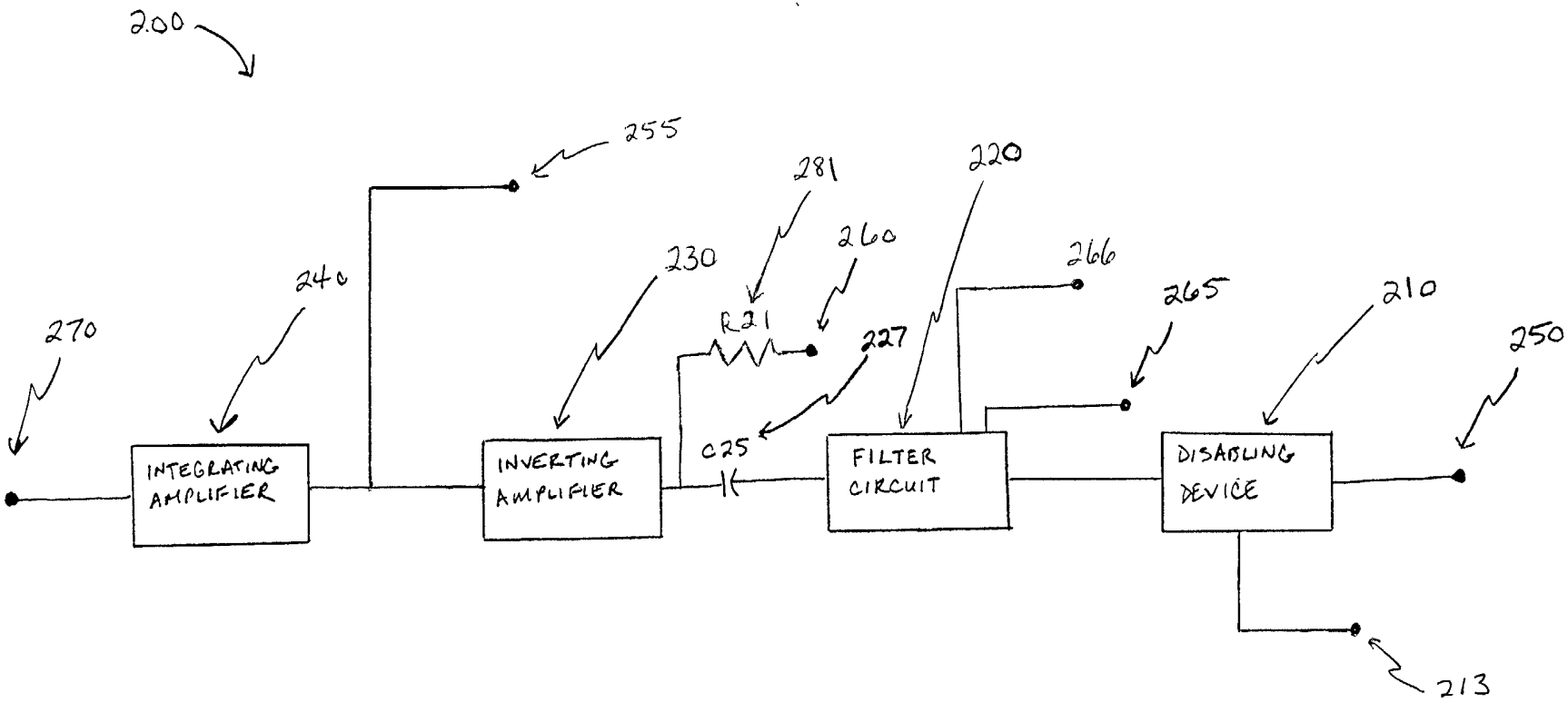
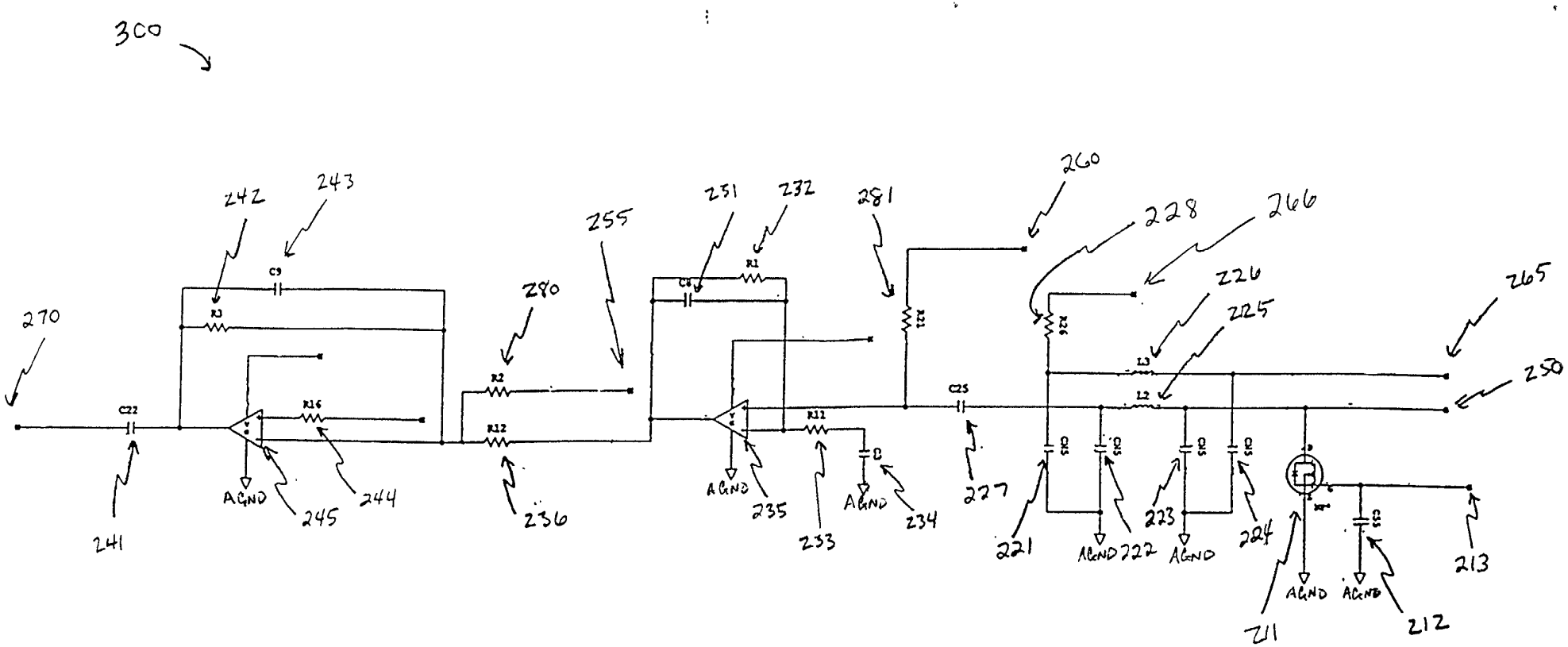


FIG. 2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C22
R3
C9
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R16
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R11
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R21
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226
225
265
250
L3
L2
C25
221
AGND
222
223
AGND
224
211
AGND
AGND
212
213

FIG. 3

DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, we hereby declare that:

Our residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

MECHANISM TO DISABLE DYNAMICALLY A COMPUTER AUDIO INPUT/OUTPUT CONNECTOR

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on ___ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			☐	☐

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Provisional Application Number	Filing Date
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Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

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